

September 23, 2001

INFORMATION DISCLOSURE STATEMENT letter

To Whom It May Concern:

The following documents are included in form PTO/SB/08A Information Disclosure Statement by Applicant as a bibliography for the application having the following title and applicant.

Title: Non-Constant Reduced-Complexity Multiplication in Signal Processing Transforms

Applicant: Charles D. Murphy

Here, the documents are discussed as they relate to the specification and claims of the application.

US Patent 6,223,197 issued to K. Kosugi on April 24, 2001 entitled "Constant multiplier, method and device for automatically providing constant multiplier and storage medium storing constant multiplier automatic providing program" discusses the notion of multiplication of two numbers in a signal processing transform when one of the numbers is a transform weight that is known and fixed. It also discusses some techniques for multiplying two numbers together, particularly with finite-precision numeric format based on power-of-two representations using binary representation elements.

This prior art patent differs from the invention of the present application in a number of ways. Claims 1, 3, and 7 of the prior art patent all specifically claim a "constant multiplier". In the present application, there is great care paid to defining constant multiplication and general multiplication. The main contribution of the present invention is a non-constant multiplier that is also not a general multiplier. In the present invention, Claims 14 and 30 represent, respectively, a machine and a method in which one of two numbers to be multiplied is a constant. However, the other number comes from a restricted set, and an implementation of the present invention can exploit the properties of the restricted set to achieve lower complexity than a constant multiplier that must be able to compute the product of the constant and any number in a particular finite-precision numeric format.

The present invention does not include a "constant decomposing section", a "minimum number of add and/or subtract terms that are each expressed as an n-th power of 2, where each n is a natural number different from that of each other add and/or subtract term", or a "minimum number of terms of positive and/or negative partial products" computed "by multiplying the multiplicand by each and every one of the add and/or subtract terms of the multiplier constant which are obtained by said constant decomposing section", all of which appear in Claim 1 of US Patent 6,223,197.

US Patent 5,903,470 issued to A. Miyoshi and T. Nishiyama on May 11, 1999 covers methods and apparatus for generating constant multiplier circuits. Claims 1, 4, 9, 11, 12, 13, 16, 21, 23, 24, 25, and 28 of this prior art all specify that one multiplier input is "a first constant represented in binary code". The invention of the present application is not a constant multiplier, however.

US Patent 5,841,684 issued to K. Dockser on November 24, 1998 discusses how to reduce the complexity of a multiplication by computing partial products and then shifting the partial products. Claim 1 specifies a "digital constant multiplication system", while claim 4 specifies a "constant multiplier system". Claim 7 specifies "a method of multiplying a multiplicand by a constant multiplier".

US Patent 5,815,422 issued to K. Dockser on September 29, 1998 is similar to US Patent 5,841,684 issued to the same inventor. In claim 1 of US Patent 5,815,422 there is "a constant multiplication device", while claim 4 recites covers "a method of multiplying a multiplicand by a constant".

US Patent 5,600,569 issued to T. Nishiyama and S. Tsubata on February 4, 1997 covers the design of multiplier circuits. It has 44 claims, which I attempt to address briefly here.

Claims 6, 11, 12, 13, 14, 15, 22, 28, 29, and 31 all specify a "constant multiplier factor A". Claims 32, 34, and 40 have a "multiplier factor A" that can be divided into the difference between a number A1 and a number A2 which are both constants, so that "multiplier factor A" is a constant. Claims 36 and 38, each for a design apparatus, and claim 40 for a multiplier do not specify whether "multiplier factor A" is a constant. However, the inventors indicate in several places that that multiplier factor A is in fact constant.

In the summary, the inventors declare:

"It is therefore an object of the present invention to provide, in the case of generating a multiplier for performing multiplication by using a constant as its multiplier factor or multiplicand and a logic circuit including such a multiplier, a method, system, and apparatus for automatically designing a logic circuit whereby a circuit having a smaller number of logic elements and logic stages can be generated and to provide a high-speed multiplier which performs multiplication by using a constant as its multiplier factor or multiplicand and which has a smaller number of logic elements and logic stages, appropriately for large-scale integration."

The inventors clearly intended in the summary that either the multiplier factor or multiplicand be a constant. Later in the patent the inventors specify:

"In Step 142 is performed a process of generating a multiplier in which a multiplier for multiplying the multiplicand X by the variable multiplier factor Y or constant multiplier factor A is converted to a circuit composed of at least one of a partial-product addition tree, an adder, and a partial-product generating circuit in accordance with a conversion rule 2."

Here, there is a clear reference to "variable multiplier factor Y" and also to "constant multiplier factor A". Finally, in the fourth paragraph from the end of the specification, the inventors state:

"In any of the above multipliers, the constant A0 is obtained by inverting all the bits in the multiplier factor A by the logic NOT operation or the constants A1 and A2 which satisfy $A=A1-A2$ are obtained, so that the multiplicand X is multiplied by the constant obtained. As a result, even if the number of all the bits in the multiplier factor A is larger than $m/2$, it is possible to maintain the number of the

partial products at $m/2$ or less, thereby reducing circuit area and increasing multiplication speed."

Claim 1 covers "a method of automatically designing a logic circuit for generating information on the logic circuit for calculating the product of a multiplier factor and a multiplicand". In claim 1, for "each bit of the multiplier factor" there are several steps. The first step (step (a) in the claim) is "judging whether the multiplier factor is a variable or a constant". Note that the result of this first step according to the claim is the same for every bit of the multiplier factor. Either the multiplier factor is a variable, or the multiplier factor is a constant. Determining whether or not individual bits of a variable multiplier factor are or are not constant is not part of step (a).

The case of the multiplier factor being a variable is relevant to the present invention.

The second step in claim 1, step (b), applies "if the multiplier factor is a variable". In this step the invention of claim 1 generates "information on a circuit for selecting, based on the value of a bit of concern in the multiplier factor, either of a signal indicating the multiplicand and a signal indicating 0" and provides "the selected signal as a partial product" output. It is not specified whether the "bit of concern" is or is not the same as the "bit of the multiplier factor" for which the steps of claim 1 are being executed.

The third step, step (c), applies "if the multiplier factor is a constant".

The fourth step, step (d), applies "if the value of said bit in the multiplier factor is 1" and involves "generating information on a circuit for outputting the signal indicating the multiplicand as a partial product". It is possible for a variable multiplier factor to have one or more bits that have constant values. The "information on a circuit" from step (d) would be provided for a multiplier factor bit that is a constant 1, and would not be provided for a multiplier factor bit that is a constant 0.

For a multiplier factor to be variable, there must be at least one bit that does not have a constant value. The fourth step does not accommodate in an explicit manner the possibility of a variable bit in a variable multiplier factor. Since the invention of claim 1 involves "the steps (a) to (e) being repeatedly executed for all the bits of the multiplier factor", step (d) prevents the invention of claim 1 from being successfully applied when the multiplier factor is variable.

Claims 2, 3, and 4 cover methods "of automatically designing a logic circuit for generating information on the logic circuit for calculating the product of a multiplier factor and a multiplicand". Each of these three claims discusses addition of partial products to ultimately produce a final product. No details are given in any of the three with respect to the constant or variable nature of the multiplier factor or the multiplicand.

Claim 5 is similar to claim 1. In particular, steps (a-1), (a-2), (a-3), (a-4), and (a-5) of claim 5 correspond to steps (a), (b), (c), (d), and (e) of claim 1 respectively. As with step (d) in claim 1, step (a-4) of claim 5 can be executed properly for a multiplier factor that is a constant or for a constant bit of a variable multiplier factor. Step (a-4) is ambiguous for variable bits of a variable multiplier factor. Since steps (a-1) through (a-5) are repeated for all of the bits of the multiplier factor, the invention according to claim 5 does not work with a variable multiplier factor.

In the opinion of the inventor of the present invention, the inventors of US Patent 5,600,569 intended that their patent cover procedures for automated design of multiplier circuits. The automated design procedures were intended to take advantage of opportunities to eliminate redundant computation when at least one of either the multiplier factor or the multiplicand happened to be constant. A large number of independent claims from the patent require specifically a "constant multiplier factor". Other claims make reference to "multiplier factor A" which in the claim is defined in terms of the difference between two constants. A few claims make reference to "multiplier factor A" without discussing whether it is constant or variable. However, these claims use the same language that in the specification is used to differentiate between constant and variable multiplier factors.

Two claims, 1 and 5, covering design procedures for multiplier circuits include steps relating specifically to constant and to variable multiplier factors. However, the invention as described in these two claims does not function properly with a variable multiplier factor. Thus US Patent 5,600,569 covers design procedures for constant multiplier circuits using binary representation elements.

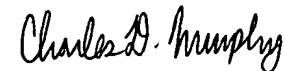
US Patent 5,159,567 issued to J. Gobert on October 27, 1992 covers multiplication by a "constant C" in each of its three claims. The constant C has a fixed number of bits, or binary representation elements. The main advantage of the invention in this patent is switching between multiplication by C and multiplication by negative C, depending on the number of non-zero bit values in each. The desired multiplication by "constant C" is implemented using multiplication by C, or bit-flipping, multiplication by negative C, and bit-flipping. Note that the invention requires a finite-precision numeric format in which negation can be implemented by bit-flipping.

Thus far, discussion of prior art has focused on constant multipliers and constant multiplication methods. General multipliers and general multiplication methods represent a large and long-standing class of prior art material. General techniques have existed and have been developed since the very beginning of digital computing. Constant multiplication techniques have become important recently due to the desire for low-cost implementation in consumer electronics devices. "Low-cost" can refer to financial cost, small size, low power consumption, or some other cost measure.

I, the inventor of the present invention have been unable to find any prior art closely similar to the material of the present invention. To the best of my knowledge, the idea of a non-constant, non-general multiplier with complexity and flexibility between those of constant and general multipliers is new and deserving of patent protection.

This concludes this INFORMATION DISCLOSURE STATEMENT letter.

Sincerely,


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		Application Number	
		Filing Date	
		First Named Inventor	Charles D. Murphy
		Group Art Unit	
		Examiner Name	
Sheet 1 of 1	Attorney Docket Number		

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Examiner Signature		Date Considered	
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